

CLAIMS

1. A process for fabricating a semiconductor substrate with a single-crystal lattice, the process comprising the steps of:

5 forming a substrate with a single-crystal lattice, the substrate having a top surface with at least one discontinuity in the single-crystal lattice therein, whereby the top surface of the substrate has a recess at the discontinuity on the top surface;

amorphizing the single-crystal lattice around a periphery of the recess;

10 depositing a layer of amorphous material having the same chemical composition as that of the substrate; and

thermally annealing the amorphous material so as to be continuous with the single-crystal lattice of the substrate.

2. The process according to claim 1, further comprising the step of:

15 planarizing the top surface of the substrate.

3. The process according to claim 2, wherein the step of planarizing the top surface includes planarizing the top surface by a chemical-mechanical polishing.

20 4. The process according to claim 1, wherein the step of forming the substrate includes forming the substrate with at least part of the material selected from the group of material consisting of silicon, germanium, silicon carbide, and gallium arsenide.

25 5. The process according to claim 3, wherein the step of amorphizing includes amorphizing with a localized ion implantation around the recess by a masking operation.

6. The process according to claim 2, wherein the step of forming a substrate include the sub-steps of:

depositing a first layer of a first material and a second layer of a second material in succession on the substrate;

etching a trench;

filling trench with a fill material so as to form the single-crystal lattice discontinuity;

etching the first layer and an upper portion of the trench fill material so as to form lateral cavities in the second layer in communication with the trench and so as to form the recess at the discontinuity; and

removing the second layer.

7. The process according to claim 6, wherein the sub-step of filling of the trench with fill material includes filling the trench with at least part of the fill material selected from the group of fill material consisting of silicon, a silicon oxide and a silicon nitride.

8. The process according to claim 6, wherein the sub-step of filling of the trench with fill material includes filling at least part of the trench with an insulating fill material.

9. The process according to claim 6, wherein the sub-step of filling of the trench is carried out by depositing silicon oxide as a conformal coating.

10. The process according to claim 6, wherein the sub-step of filling of the trench is carried out by thermal oxidation of the silicon.

11. The process according to claim 6, wherein the sub-step of etching includes forming a buried capacitor in the trench.

12. The process according to claim 11, wherein the sub-step of etching the trench includes etching a trench with walls and wherein the sub-step of filling the trench further comprises:
lining the walls of the trench with oxide by thermal oxidation;
depositing a highly doped polycrystalline silicon in the trench so as to fill it; and
etching the polycrystalline silicon so that a fill level of the trench is below the surface of the substrate.

13. The process according to claim 6, wherein the sub-step of etching includes forming a buried diode in the trench.

14. The process according to claim 13, wherein the sub-step of filling the trench further comprises:
depositing a highly doped polycrystalline silicon in the trench so as to fill it; and
etching the polycrystalline silicon so that a fill level of the trench is below the surface of the substrate.

15. The process according to claim 6, wherein the step of amorphizing includes amorphizing the single-crystal lattice around a periphery of the recess so as to be self-aligned with the trench.

16. The process according to claim 14, wherein the step of amorphizing includes amorphizing the single-crystal lattice around a periphery of the recess so as to be self-aligned with the trench.

Parameter	1990-1995	1996-2000	2001-2005	2006-2009	2010-2014	2015-2019	2020-2024	2025-2029	2030-2034	2035-2039	2040-2044	2045-2049	2050-2054	2055-2059	2060-2064	2065-2069	2070-2074	2075-2079	2080-2084	2085-2089	2090-2094	2095-2099	2100-2104	2105-2109	2110-2114	2115-2119	2120-2124	2125-2129	2130-2134	2135-2139	2140-2144	2145-2149	2150-2154	2155-2159	2160-2164	2165-2169	2170-2174	2175-2179	2180-2184	2185-2189	2190-2194	2195-2199	2200-2204	2205-2209	2210-2214	2215-2219	2220-2224	2225-2229	2230-2234	2235-2239	2240-2244	2245-2249	2250-2254	2255-2259	2260-2264	2265-2269	2270-2274	2275-2279	2280-2284	2285-2289	2290-2294	2295-2299	2300-2304	2305-2309	2310-2314	2315-2319	2320-2324	2325-2329	2330-2334	2335-2339	2340-2344	2345-2349	2350-2354	2355-2359	2360-2364	2365-2369	2370-2374	2375-2379	2380-2384	2385-2389	2390-2394	2395-2399	2400-2404	2405-2409	2410-2414	2415-2419	2420-2424	2425-2429	2430-2434	2435-2439	2440-2444	2445-2449	2450-2454	2455-2459	2460-2464	2465-2469	2470-2474	2475-2479	2480-2484	2485-2489	2490-2494	2495-2499	2500-2504	2505-2509	2510-2514	2515-2519	2520-2524	2525-2529	2530-2534	2535-2539	2540-2544	2545-2549	2550-2554	2555-2559	2560-2564	2565-2569	2570-2574	2575-2579	2580-2584	2585-2589	2590-2594	2595-2599	2600-2604	2605-2609	2610-2614	2615-2619	2620-2624	2625-2629	2630-2634	2635-2639	2640-2644	2645-2649	2650-2654	2655-2659	2660-2664	2665-2669	2670-2674	2675-2679	2680-2684	2685-2689	2690-2694	2695-2699	2700-2704	2705-2709	2710-2714	2715-2719	2720-2724	2725-2729	2730-2734	2735-2739	2740-2744	2745-2749	2750-2754	2755-2759	2760-2764	2765-2769	2770-2774	2775-2779	2780-2784	2785-2789	2790-2794	2795-2799	2800-2804	2805-2809	2810-2814	2815-2819	2820-2824	2825-2829	2830-2834	2835-2839	2840-2844	2845-2849	2850-2854	2855-2859	2860-2864	2865-2869	2870-2874	2875-2879	2880-2884	2885-2889	2890-2894	2895-2899	2900-2904	2905-2909	2910-2914	2915-2919	2920-2924	2925-2929	2930-2934	2935-2939	2940-2944	2945-2949	2950-2954	2955-2959	2960-2964	2965-2969	2970-2974	2975-2979	2980-2984	2985-2989	2990-2994	2995-2999	3000-3004	3005-3009	3010-3014	3015-3019	3020-3024	3025-3029	3030-3034	3035-3039	3040-3044	3045-3049	3050-3054	3055-3059	3060-3064	3065-3069	3070-3074	3075-3079	3080-3084	3085-3089	3090-3094	3095-3099	3100-3104	3105-3109	3110-3114	3115-3119	3120-3124	3125-3129	3130-3134	3135-3139	3140-3144	3145-3149	3150-3154	3155-3159	3160-3164	3165-3169	3170-3174	3175-3179	3180-3184	3185-3189	3190-3194	3195-3199	3200-3204	3205-3209	3210-3214	3215-3219	3220-3224	3225-3229	3230-3234	3235-3239	3240-3244	3245-3249	3250-3254	3255-3259	3260-3264	3265-3269	3270-3274	3275-3279	3280-3284	3285-3289	3290-3294	3295-3299	3300-3304	3305-3309	3310-3314	3315-3319	3320-3324	3325-3329	3330-3334	3335-3339	3340-3344	3345-3349</
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Docket No. 00-GR1-239

18. An integrated circuit comprising:

a silicon substrate with a single-crystal lattice, the substrate having a top surface with at least one discontinuity in the single-crystal lattice therein, whereby the top surface of the substrate has a recess at the discontinuity on the top surface, wherein the single-crystal lattice is amorphized around a periphery of the recess; and

a layer of amorphous material having the same chemical composition as that of the substrate is deposited on the single-crystal lattice which has been amorphized, whereby the amorphous material is thermally annealed so as to be continuous with the single-crystal lattice of the substrate.

19. The integrated circuit according to claim 18, further comprising at least two adjacent transistors formed within the substrate comprising at least one buried trench and the surface of which is made uniform in accordance with the process according to claim 6, the trench forming an isolating trench separating the contiguous buried layers of the transistors.